The Examiner has rejected claims 1-18 under 35 U.S.C. §103(a) as being unpatentable over Cole et al., U.S. Patent No. 5,548,223, (hereinafter "Cole") in view of King and Elder.

Claims 1-18 were originally presented for Examination. Claim 3 has been canceled by way of the present Response. Claim 1 has been amended by way of the present Response. Claims 1, 2 and 4-18 are currently pending, of which, claim 1 is in independent form. Favorable reconsideration of the present amendment as currently constituted is respectfully requested.

Regarding the Attorney Docket Number

Applicant has amended the Attorney Docket Number for the present application to be consistent with the undersigned's office practice. Applicant respectfully requests that the PTO records be amended accordingly.

Regarding the Rejections Under 35 U.S.C. §102(b)

Claims 1, 2 and 10-12 stand rejected under 35 U.S.C. §102(b) as being anticipated by King. The present invention, as defined by amended independent claim 1, is directed to a method for manufacturing a wafer-interposer assembly. The method includes the step of providing a semiconductor wafer including one or more semiconductor die wherein each semiconductor die includes one or more first electrical contact pads. An interposer having one or

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more communication interfaces and a second electrical contact pad corresponding to each of the one or more first electrical contact pads on each semiconductor die of the semiconductor wafer is provided. The wafer-interposer assembly is formed by connecting each first electrical contact pad of the semiconductor wafer to the corresponding second electrical contact pad of the interposer with a conductive attachment element. In particular, the wafer-interposer assembly is singulated into one or more chip assemblies each of which includes a chip and a section of the interposer. Prior to singulation, the wafer-interposer assembly allows for the "simultaneous or near simultaneous testing [of] multiple wafer-interposer assemblies. As a result, the number of manufacturing operations are reduced, thereby improving first pass yields." Specification, page 11, lines 10-13.

Applicant respectfully submits that King neither discloses nor suggests Applicant's invention as recited in amended claim 1. In particular, King neither discloses nor suggests singulating a wafer-interposer assembly formed by connecting the semiconductor wafer to the interposer. King discloses a method for probe testing and burning-in of integrated circuits formed within chips on a silicon wafer by attaching an integrator substrate to the silicon wafer. After testing, the integrator is either removed from the silicon wafer so that the silicon wafer may be conventionally diced and so that the individual chips may be conventionally packaged or

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the silicon wafer and an integrator are formed into a wafer scale package. King describes his method for testing, burning-in and manufacturing as follows:

> If all of the die on the wafer test out to be good, then the complete wafer 12 is transferred via path 24 to an assembly station 26 where the complete wafer and integrator are packaged for shipment to the customer. If, however, only a partial or fractional number of the die on the wafer test out to be good, but this number is still above the threshold yield requirement for a given wafer scale application, then the wafer 12 is removed from the integrator 18 and transported via path 28 to the station 30 where the wafer 12 is trimmed to size with all the good die thereon left intact and then matched in station 32 to the correct matching integrator pattern. The integrator 18 is then programmed in station 34 to blow the appropriate fuses on the wafer cluster remaining at station 32 for a given partial array application. The combination wafer and integrator is then transferred via path 36 to a final packaging station 38. In the final packaging station 38, the combination wafer and integrator may either be: (1) installed in a prefabricated case having external plug connections; or (2) it may be encapsulated using fluidized bed encapsulation, or (3) it may be encapsulated in a package using transfer molding encapsulation, or (4) it may be "potted" in a curable compound.
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> On the other hand, if the die yields do not meet certain threshold requirements for either a full or partial wafer scale application, then the wafer is separated from the integrator and transferred via path 40 to a standard component production operation as indicated at station 42, after which the wafers are diced at a conventional wafer dicing station 44. The dice are then assembled at station 46 into plastic or ceramic single die packages. Column 5, lines 18-50.

As illustrated in figure 1 and described by King, the goal of the King method is to create wafer scale packages that include a fully or partially integrated wafer. If it is determined that the wafer yield is insufficient for wafer scale packaging, however,

then the wafer is separated from the integrator for dicing and single die packaging. Accordingly, the King method neither discloses nor suggests Applicant's method for manufacturing a wafer-interposer assembly as recited in claim 1. Applicant respectfully requests withdrawal of the outstanding §102(b) rejection and allowance of claim 1.

Claims 2 and 10-12 depend from independent claim 1 and introduce further limitations in combination therewith. Therefore, the allowance of claims 2 and 10-12 is respectfully requested.

Claims 1, 2 and 10-12 stand rejected under 35 U.S.C. §102(b) as being anticipated by Elder. The present invention, as defined by amended claim 1, is directed to a wafer-interposer assembly constructed of a wafer and interposer wherein assembly is "accomplished through creating a set of permanent electrical and mechanical connections between the wafer and the interposer using the conductive attachment elements." Specification, page 14, lines 1-3. Applicant's construction eliminates the need for standard test equipment such as probes. Specification, page 13, lines 20-21. Applicant respectfully submits that Elder neither discloses nor suggests Applicant's invention as recited in claim 1. In particular, Elder neither discloses nor suggests a method for manufacturing a wafer-interposer assembly that comprises a semiconductor wafer including one or more semiconductor die as recited by Applicant.

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Elder discloses a burn-in test socket which serves as a temporary package for integrated circuit die. As seen in figure 1, the burn-in test socket of Elder tests singulated, individual die that have already been cut from a wafer. The Elder burn-in test socket is not a wafer level device like Applicant's wafer-interposer assembly. Elder describes his burn-in test socket as follows:

> Heat sink 22 has a plurality of fingers 23 on the top thereof to help dissipate heat from semiconductor die 21, which is mounted in cavity 30 in the heat sink. When heat sink 22 and probe head 17 are brought into contact with each other, the cavity 30 holds semiconductor die 21 in place, and the test pads thereon (not illustrated) contact the bumps 24 on probe head 17. Column 3, lines 31-37.

As described by Elder, the burn-in test socket temporarily tests semiconductor die via a probe. Therefore, the testing scheme of Elder does not disclose or suggest Applicant's invention as recited in claim 1 wherein a wafer-interposer assembly provides for the testing of semiconductor dies without a probe. Accordingly, Applicant respectfully requests withdrawal of the outstanding §102(b) rejection and allowance of claim 1.

Claims 2 and 10-12 depend from independent claim 1 and introduce further limitations in combination therewith. Therefore, the allowance of claims 2 and 10-12 is respectfully requested.

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Regarding the Rejection Under 35 U.S.C. §103(a)

Claims 1-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Cole in view of King and Elder. Applicant respectfully submits that the deficiencies of King and Elder are not overcome by Cole. Cole neither discloses nor suggests a method for manufacturing a wafer-interposer assembly that provides for the wafer level testing of chips on a semiconductor wafer formed into a wafer-interposer assembly. Cole discloses a test fixture that aids in the testing of packaged semiconductor die, not chips on a semiconductor wafer formed into a wafer-interposer assembly as recited by Applicant. Additionally, with reference to figure 1, the flexible dielectric substrate 12 of Cole is not an interposer, but a portion of adapter 10 testing equipment that tests SMT, PGA and hybrid devices. Cole describes his testing equipment as follows:

> Referring to FIG. 1, there is shown an adapter 10 for an electrical test probe according to the present invention. The adapter 10 has a flexible dielectric substrate 12 with electrically conductive runs 14 formed thereon. Electrical contacts 16 are formed on one end of the conductive runs 14 adjacent to a first edge surface 18 of the dielectric substrate 12. Electrical contacts 20 are also formed on the other end of runs 14 adjacent to a second edge surface 22 of substrate 12 opposite the first edge surface 18. The side surfaces 24 and 26 of the substrate angle outward from the first edge surface 18 to the second edge surface 22 forming a substantially trapezoidal shaped adapter 10.
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> The adapter 10 is designed to interface with electrical contacts or leads 28 of electronic devices 30, such as surface mounted integrated circuit devices (SMT), pin-

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grid-array (PGA) devices, and hybrid devices. Column 3, lines 28-43.

As described by Cole, the adapter 10 is designed to interface with packaged semiconductor die as a testing apparatus and does not form an wafer-interposer assembly with a semiconductor wafer. Accordingly, Cole neither discloses nor suggests Applicant's claimed invention.

Moreover, Applicant's claimed invention is not found in the combination of Cole and King. Assuming *arguendo* that Cole and King could be combined as described by the Examiner, a wafer-interposer assembly constructed of an interposer and semiconductor wafer that is singulated would not be found. As previously discussed, Cole does do not disclose an interposer and the King manufacturing method neither discloses nor suggests Applicant's wafer-interposer assembly. The combination of Cole and King yields a process wherein following the wafer level testing of chips on the King wafer, which is coupled to an integrator, and a determination that the wafer has an insufficient yield, the wafer and integrator are deconstruction, the wafer is singulated into individual die and each die is individually retested by the probe adapter of Cole. Accordingly, the method as recited in claim 1 is not found in the combination of Cole and King.

Furthermore, Applicant's claimed invention is not found in the combination of Cole and Elder. Assuming *arguendo* that Cole and Elder could be combined as described by the Examiner, a wafer-

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interposer assembly constructed of an interposer and semiconductor wafer would not be found. As previously discussed, Cole does not disclose an interposer and the testing scheme of Elder does not disclose or suggest an interposer that provides for the wafer level testing of chips on a semiconductor wafer formed into a wafer-interposer assembly. The combination of Cole and Elder yields a process for testing die that provides for individual die testing by either a Cole probe adapter or an Elder socket. Hence, Applicant's method is not found in the combination of Cole and Elder.

Accordingly, Applicant respectfully requests withdrawal of the outstanding §103(a) rejection and allowance of claim 1. Claim 3 has been cancelled and claims 2 and 4-18 depend from independent claim 1 and introduce further limitations in combination therewith. Therefore, the allowance of claims 2 and 4-18 is respectfully requested.

Fee Statement

Form PTO-2038 is submitted herewith authorizing the Commissioner to charge $460.00 to the indicated account for an Extension for Response within Third Month per 37 C.F.R. §1.17(a)(3). The total number of claims has been reduced and number of independent claims remains unchanged. Accordingly, Applicant believes no additional fees are due for the filing of this Response. If any additional fees are due, however, or any

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overpayments have been made, please charge, or credit, our Deposit Account No. 03-1130.

The Examiner is requested to call the undersigned for any reason that would advance the instant application to issue.

Dated this 15th day of November, 2002.

Respectfully submitted:

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Marked Up Claims per 37 C.F.R. §1.121(c)(1)(ii)

1. (Amended) A method for manufacturing a wafer-interposer assembly comprising the steps of:

providing a semiconductor wafer including one or more semiconductor die, each semiconductor die having one or more first electrical contact pads;

providing an interposer having one or more communication interfaces and a second electrical contact pad corresponding to each of the one or more first electrical contact pads on each semiconductor die of the semiconductor wafer, and at least one of the second electrical contact pads electrically connected to the one or more communication interfaces; [and]

forming the wafer-interposer assembly by connecting each first electrical contact pad of the semiconductor wafer to the corresponding second electrical contact pad of the interposer with a conductive attachment element; and

singulating the wafer-interposer assembly into one or more chip assemblies.